Lab 05

Adders/Subtractor

ECE 380-002

University of Alabama

Yichen Huang

Thomas Dillman

2019/09/30

**Introduction**

In this lab, we used the Quartus II software package to design and simulate behavioral adder, ripple carry adder, and LPM\_ADD\_SUB implementation. We also printed the Mega function schematic or VHDL files for Designs A, B, and C.

**Procedure**

1. Prelab
2. Design A

A screenshot of a cell phone

Description automatically generatedIn the design A, we created a project in the software and make a VHDL file called adder4a.vhd. We type the dataflow VHDL in the file. Then we run the compile, after compiling successfully, we run the test file and run different case in waveform file.

A picture containing screenshot

Description automatically generated

1. Design B

In the design B, we created a new project and implement a 4-bit ripple adder using structural VHDL. We created two files ‘fulladd.vhd’ and ‘adder4.vhd’. After implementation, we compile two files. Finally, we run the test file through waveform file. We group 4 single bits for input X, Y and output S.

A screenshot of a computer

Description automatically generatedA screenshot of a social media post

Description automatically generatedA screenshot of a social media post

Description automatically generated

1. Design C

A screenshot of a computer

Description automatically generatedIn the design C, we implement a 4-bit adder using the LPM\_ADD\_SUUB module in the schematic file ‘adder4c.bdf’. The circuit has 2 4-bits data input, a carry-in bit, a add or sub control input and a 4-bit data output, a carry-out output and an overflow output. After we finish the schematic, we run the compiling process.

1. During the lab
2. Design A

In the project of designA, we set the switches on the DE1 board. After setting, we recompile again. Then we upload the project to the DE1 board, after configuration, we test the case on the board again, the result is same in the A screenshot of a video game

Description automatically generatedprelab.

1. Design B

In the design B, we repeat the process in design A again; after setting the DE1 board, we compile the project again and upload the file to the DE1 board. Finally, we upload the file to the DE1 board. After setting, we stimulate the test again on the board by turn on or turn off the switch. The result is same as the prelab stimulation.

A screenshot of a computer

Description automatically generated

1. A screenshot of a cell phone

   Description automatically generatedDesign C

A screenshot of a computer

Description automatically generatedA screenshot of a video game

Description automatically generatedIn design C, we firstly run the stimulation by the waveform file. We repeat the setting DE1 board process same as Design A and B. Then, we run the compiling process again and upload the file to the DE1 board. After configuration, we do the testing process. The result is same as the result of waveform file.

A screenshot of a social media post

Description automatically generated

**Result**

The result of design A and B are same as the waveform result in the prelab. For the design C, the final result is also same as the waveform file result.

A close up of a piece of paper

Description automatically generated

**Conclusion**

In this lab, we learned two different ways to build an adder in VHDL file. We also understand the method to test the adder. Furthermore, we also learned how to insert ADD\_SUB Gate to the schematic file.

A close up of text on a white background

Description automatically generated